REMARKS

The present Response is submitted in response to the Office Action dated August 13, 2003, where the Examiner has ***finally rejected*** claims 1-20 pending in the present application. Reconsideration and allowance of pending claims 1-20 in view of the following remarks are respectfully requested.

A. Rejection of Claims 1-20 Under 35 USC §102

The Examiner has rejected claims 1-20 under 35 USC §102(b) as being anticipated by Merrill, et al. (USPN 5,886,393) ("Merrill '393"). Applicant respectfully disagrees and submits that the present invention, as defined by independent claims 1, 8 and 15, is patentably distinguishable over Merrill '393.

Independent claims 1, 8 and 15, are directed to an off-chip inductor, wherein the inductance of the bonding wire, i.e., the inductor, is defined by a first selected dimension of said bonding wire, wherein "said first selected dimension is measured along a first axis substantially perpendicular to said top surface of said semiconductor die." By way of clarification, applicant references Figure 1 of the present application, which illustrates, in perspective view, exemplary structure 100 including inductor 116, which comprises bonding wire 118, stud bump 120 and ball bump 122. As shown in Figure 1, the length of bond wire 118 is determined by distance 130 and loop height 128. While distance 130 corresponds to "the distance between the centers of semiconductor die bond pad 124 and semiconductor die bond pad 126," (page 10, lines 3-4 of the present application) loop height 128 corresponds to "the distance between the apex of bonding wire 118 and top

surface 114 of semiconductor die 102." Page 9, lines 22-23 of the present application. Thus, bonding wire 118 extends from top surface 114 of semiconductor die 102 to an "apex" defining an axis substantially perpendicular to top surface 114 of semiconductor die 102. Loop height 128, therefore, corresponds to a dimension measured along an axis substantially perpendicular to top surface 114 of semiconductor die 102, as specified by claims 1, 8 and 15.

Among other advantages, this unique arrangement "takes advantage of the space freely available on the top surface of the semiconductor die which space is otherwise not utilized." Page 12, lines 14-16 of the present application. Moreover, this free space on the top surface of the semiconductor die is advantageously utilized in both an axis (and, similarly, a planar surface) parallel to the top surface of semiconductor die, such as distance 130, and an axis (and, similarly, a planar surface) substantially perpendicular to the top surface of the semiconductor die, such as loop height 128. For the reasons that follow, applicant respectfully submits that Merrill '393 fails to disclose or suggest such an arrangement.

Initially, applicant notes that the Examiner incorrectly states that "the applicant states in his remarks on page 8, second paragraph that Merrill teaches wherein an inductance of the inductor is increase [sic] by increasing a loop height of the bonding wires 173a-173d, and wherein decreasing the loop height of the bonding wire decreases the inductance of the inductor" as stated on pages 2 and 4 of the Detailed Action. Quite the contrary, with reference to page 8, second paragraph of the Response filed by the applicant on May 19, 2003, applicant states that "Merrill '393, however, does not disclose

or suggest controlling inductance by selection of a loop height. Instead, Merrill '393 provides that the inductance is determined by the bond wire length, not the bond wire height (see, e.g., col. 5, lines 5-8)."

Continuing with the disclosure of Merrill '393, applicant respectfully submits that Merrill '393 fails to disclose that the inductance of the inductor is defined by a first selected dimension of said bonding wire, wherein "said first selected dimension is measured along a first axis substantially perpendicular to said top surface of said semiconductor die," contrary to the Examiner's conclusion as set forth in the present Office Action. The Examiner relies on the Col. 5, lines 5-35 of Merrill '393, which describes the inductor loops shown in Figures 2 and 3 of Merrill '393. Specifically, the Examiner notes that each of the inductor loops shown in Figures 2 and 3 of Merrill '393 define an area enclosed by the inductor loop. However, the inductor loops and the area defined by the inductor loops shown in Figure 2 and 3 of Merrill '393 lie on a plane which is parallel to, and not perpendicular to, the top surface of the die.

Moreover, Merrill '393 fails to disclose a "loop height" corresponding to a dimension of the inductor loop which is measured from the top surface of the die to an "apex" of the inductor loop, i.e., a dimension "measured along a first axis substantially perpendicular to said top surface of said semiconductor die." As such, Merrill '393 neither discloses nor suggests a "loop height" in accordance with the present application.

Furthermore, even assuming a "loop height" could be established with regard to the inductor loops described in Merrill '393, such a "loop height" would be measured along an axis (or plane) which is parallel to the top surface of the die, and not along a

dimension of the inductor loop which is measured from the top surface of the die to an "apex" of the inductor loop. This is because, as noted above, the inductor loops in Merrill '393 define an area which lies on a plane which is parallel to the top surface of the die. For example, Merrill '393 discloses various embodiments, wherein the inductance of the bond wire is strictly controlled by the distances between bonding terminals pad, e.g., bonding terminal pads 172a, 172b, 172c and 172d in Figure 5 of Merrill '393. Thus, the inductance of bonding wire 173a, for example, corresponds to the distance between bonding terminal pads 172a and 172b, where distance between bonding terminal pads 172a and 172b is measured along an axis parallel to the surface of die 128. Consequently, Merrill '393 is strictly limited to controlling inductance by a dimensional axis (or plane) parallel to the surface of die 128, and neither discloses nor suggests that the inductance of the inductor is determined and controlled by means of a first selected dimension that is measured along an axis substantially perpendicular to said top surface of said semiconductor die. Any "loop height" established in Merrill '393 would thus fail to amount to a "dimension is measured along a first axis substantially perpendicular to said top surface of said semiconductor die" as specified by claims 1, 8 and 15.

In sum, Merrill '393 discloses an inductor arrangement wherein the length of the inductor is measured along an axis (or plane) parallel to, and not perpendicular to, the top surface of a semiconductor die, and, therefore, fails to disclose or suggest the off-chip inductor specified by claims 1, 8 and 15. Accordingly, applicant respectfully submits that the rejection of independent claim 1 and its corresponding dependent claims 2-7, independent claim 8 and its corresponding dependent claims 9-14, and independent claim

15 and its corresponding dependent claims 16-20 has been traversed, and therefore, claims 1-20 should be allowed.

B. Conclusion

For all the foregoing reasons, allowance of claims 1-20 pending in the present application is respectfully requested.

Respectfully Submitted;
FARJAMI & FARJAMI LLP

Dated: 10/30/03

Michael Farjami, Esq.
Reg. No. 38,135

Michael Farjami, Esq.
FARJAMI & FARJAMI LLP
16148 Sand Canyon
Irvine, California 92618
Tel: (949) 784-4600
Fax: (949) 784-4601

CERTIFICATE OF MAILING
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed: Mail Stop AF, Commissioner for Patents P.O. Box 1450, Alexandria, VA 22313-1450

Date of Deposit: 10/30/03

Lori Lbave
Name of Person Mailing Paper and/or Fee

Signature 10/30/03
Date